A High Efficiency GaAs Power Amplifier Module with a Single Voltage for Digital Cellular Phone Systems

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Abstract

This work describes a two-stage 0.2 cc power amplifier (PA) module with single voltage operation for digital cellular phone system terminals. A new GaAs FET structure enables this operation. To increase power-added efficiency, it is found to be advantageous to use heat spreading with a Cu plate in the cavity and second-order harmonic suppression with the trap capacitor built into the drain bias circuit. Output power of 30.5 dBm with power added efficiency of 54% has been obtained at 1.45 GHz and 3.5 V.

Introduction

Recently, digital cellular phone system terminals such as PDC have required large reductions in size and weight. Power amplifiers in them have required low power consumption in addition to above things. 0.2 cc PA modules and FETs have been reported [1] [2], however, these need negative voltages such as an external DC-DC converter in order to run on batteries. Therefore, modules that do not operate on negative voltage are now much needed to further reduce the size of terminals. High efficiency modules are also required to save batteries.

We propose the following technologies to achieve the two-stage 0.2 cc PA module with single voltage operation.

(1) A new FET structure for single-voltage operation.

(2) Thermal via, cavity structure and inter-metal between the FET and substrate to reduce heat resistance.

(3) Second-order harmonic suppression using a trap capacitor built into the bias circuit.

This PA module not only facilitates miniaturization by connecting to the PDC terminals with a single voltage, but it also has fewer parts since it no longer needs an FET gate bias circuit.

Device Characteristics

The first step in bringing about single voltage operation was to improve the GaAs FET [3]. PAs generally use FETs with deep pinch-off voltages (Vp) and apply negative gate voltage (Vg) in order to generate high output power. When the gate is connected to the ground, power-added efficiency drops because of an increase in operating current. An FET is therefore needed when Vp is shallow and a gate forward voltage (Vf) is large. This led us to develop an FET with a large maximum drain current (Idmax), which we accomplished by using Pt metal for the gate electrode. As a result, an Idmax of more than five times the drain saturation current (Idss) of 50 mA/mm was achieved. The maximum transconductance (gm) was 330 mS/mm, and Vp was -0.4 V with a drain voltage of 3.5 V.

Heat Resistance Reduction

The circuit components must fit into a 10-mm square area in order to achieve a module of 0.2 cc volume. Because it is not easy with a two-stage amplifier using a single-layer substrate, we used a multi-layer substrate instead. Losses were reduced by

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using a glass ceramic substrate that permitted the use of low-metal resistance Ag (3 m Ω/□).

Unfortunately the substrate had poor thermal conductivity at 2.5 W/m · K. Therefore a better means of spreading heat from the FET had to be found. We used thermal via to spread heat better, a cavity structure to reduce the thickness of the substrate directly below the FET, and then inserted a 0.5-mm-thick Cu plate between the FET and the substrate to reduce thermal resistance.

Figure 1 shows the Cu plate and GaAs FETs in the cavity. The thermal resistance of the module without the plate was 34 K/W and that with the plate was 19 K/W from measurement results. The effect of the plate was to reduce thermal resistance by 40%. This level of thermal resistance was better than that of aluminum ceramic substrate without the plate.

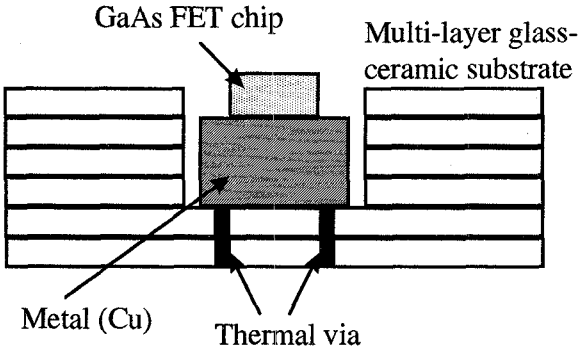

Figure 1 Cu plate and GaAs FET in the cavity

Second-Order Harmonic Suppression

To lower the second-order harmonic output power, a trap capacitor is built into the bias circuit which is in an output matching circuit. Figure 2 shows the output matching circuit. In general, a λ/4 microstrip line is used at a bias circuit. The impedance of the λ/4 microstrip line on a substrate is usually open at fundamental frequency f0 (1.45 GHz), but is not shorted at the second-order harmonic frequency 2f0 (2.9 GHz). This is because the wavelength compression rate of the line depends on frequency, and it is hard to control the line length on the substrate. If the second-order harmonic is not perfectly shorted, this spurious power appears in the output terminal.

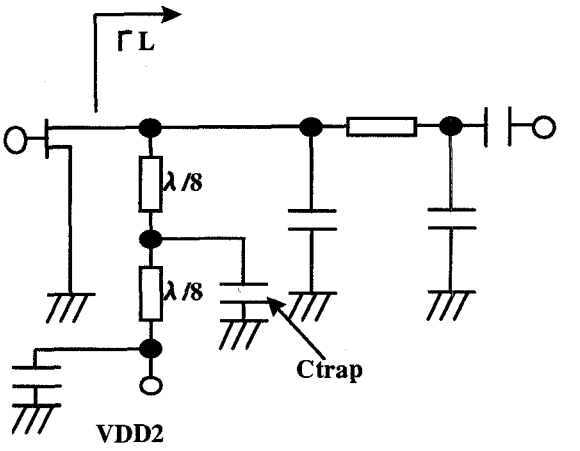

Figure 2 A trap capacitor built into the bias circuit

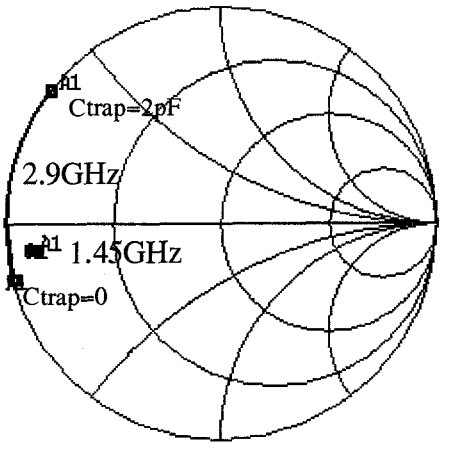

Figure 3 Trap capacitance dependence of load impedance (Γ L) at f0 and 2f0

This problem was resolved by placing a trap capacitor in the middle of the λ/4 microstrip line. Since the series inductance of the capacitor is about 1 nH, this is basically the same as no capacitor at f0 in the case of small capacitance. At 2f0 however, this cannot be negligible because of low impedance. Figure 3 shows trap capacitance dependence of load

impedance at f0 and 2f0 varying capacitance from 0 to 2 pF. Load impedance at f0 is the same at any trap capacitance, but that at 2f0 can be changed by adequately choosing capacitance. We found with a 1 pF trap capacitor that a gain suppression at 2f0 was 10 dB better than without the trap capacitor.

One feature of the module is that we devised a layout where the trap circuit takes up no space.

Module Circuit Structure

Figure 4 shows a circuit diagram of the PA module. The chip gate widths and sizes are 1.6 mm and 0.8 x 0.7 mm on the first stage FET, and 8.16 mm and 0.8 x 1.04 mm on the second stage FET, respectively. Both FETs are at class AB operating mode, very close to class B.

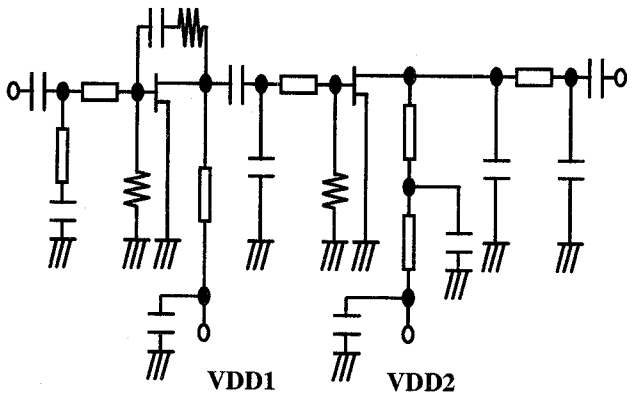

Figure 4 A circuit diagram of the PA module

Optimum input and output impedance for output power and distortion at each FET stage were determined using source and load pull methods, and circuit parameters such as capacitance were later optimized through circuit simulations. The first-stage FET, with a small stability factor due to a short gate width, tended to oscillate, but stability was improved by inserting a feedback circuit comprised of a resistor and capacitor.

Losses due to the conductive resistance of the microstrip line also negatively affect module performance. Therefore the drain bias and output matching circuits of the second-stage FET were placed on the top layer, and other circuits were placed on the inner layer. Passive circuit components were consisted of 11 chip capacitors and 3 chip resistors. At least 6 components (4 resistors and 2 capacitors) were needed in the gate bias circuit with a two-voltage configuration, but four of them (2 resistors and 2 capacitors) were unnecessary in this module. Figure 5 shows the top view of the PA module. The resistance of the second drain bias circuit was less than 0.07 Ω.

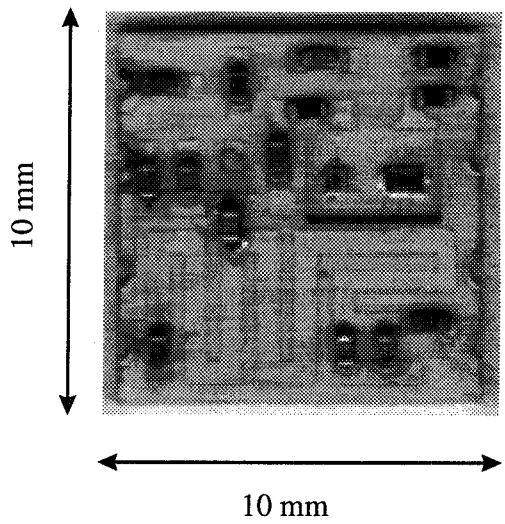

Figure 5 Top view of the PA module

Measured Results

Figure 6 compares small signal gain with and without trap capacitance (Ctrap=2 pF) from 1.0 GHz to 3.0 GHz. The gain of the second-order harmonic frequency, 2.9 GHz, was suppressed about 10 dB. The same result was obtained for large signal characteristics. The second-order harmonic output power was 40.0 dBc less than at the fundamental frequency, and was 10 dB better with the trap capacitor than without it, as is shown in figure 7. When measurements of the module were taken, the two-stage amplifier yielded output power of 30.5 dBm with power-added efficiency of 54% at 1.45 GHz and 3.5 V, as is shown in figure 8. The input power and an operating current were 7dBm and 582 mA,

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respectively.

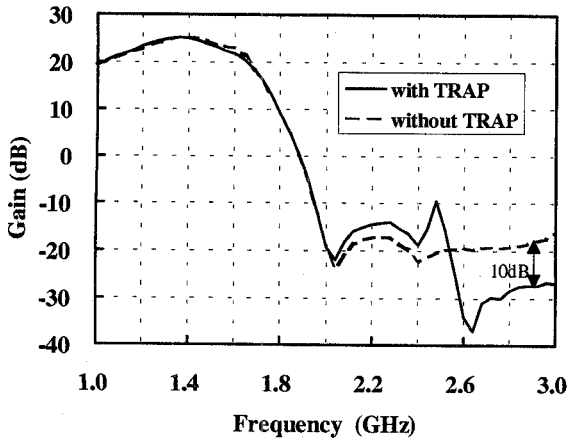

Figure 6 Comparison of small signal gain with and without a trap circuit

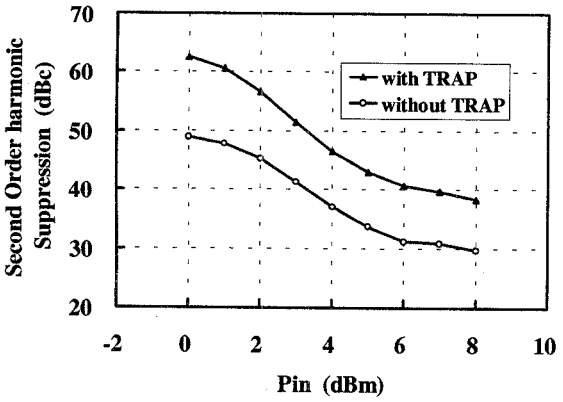

Figure 7 Comparison of second-order harmonic suppression with and without a trap circuit

Conclusion

FETs with single voltage operation were obtained by using Pt metal for the gate electrode. The 0.2 cc power amplifier module achieved an output power of 30.5 dBm with power-added efficiency of 54% at 1.45 GHz and second-order harmonic power of 40 dBc at 3.5 V. Heat spreading with a Cu plate in the cavity and second-order harmonic suppression with the trap capacitor largely contributed to this high performance. This work is the first single-voltage module to exhibit performance on a par with two-voltage modules using FETs.

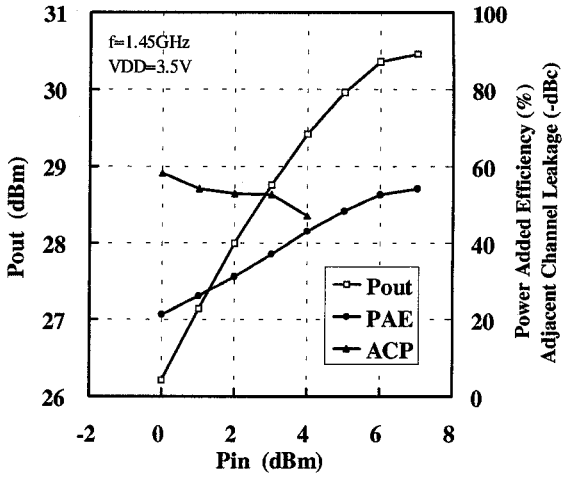

Figure 8 Measured input-output characteristics of the 0.2 cc PA module

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